Hybrid Silicon Photonics for High-Speed Optical Interconnect
July 2014
Overview

Silicon Photonics: Introduction

Silicon Photonics Technology Platform

Light Source for Silicon Photonics

Silicon Photonics Transceiver Systems

Silicon Photonics Technology Scaling

Applications for Silicon Photonics Transceivers
Silicon Photonics: Introduction

• **Silicon Photonics Technology:**
  - Silicon material system & processing techniques to manufacture integrated optical circuits and devices
  - Passive optics + optical modulation + optical detection (+ electronic circuits)

• **Goal of Silicon Photonics:**
  - Leverage from the IC industry:
    - Design infrastructure and methodologies
    - Wafer manufacturing and methodologies
    - Packaging & Test infrastructure and methodologies
  - Enable a high level of integration:
    - Increased functionality and density
    - Simplification of optical/electrical packaging & test

• **Silicon Photonics Applications:**
  - Most silicon photonics applications in high-speed communications
  - Emerging applications in areas of biochemistry and motion sensors
Silicon Photonics: Process Technology

- **Substrate:** SOI (~300 nm Si body, ~720/800 nm BOX)
- **Optical trench:**
  - 193 nm litho for very fine structures
  - Critical CD and etch depth control
- **Implants:** standard
- **Selective Epitaxy of 100% Ge**
- **Contacts:** Single contact process for Si and Ge
- **4-6 metal layers**
200 mm Si Photonics process (mature)
- Freescale Semiconductor (Austin, TX)
- Monolithic integration electronics/photonics
- Extensive electronic and photonic device library
- Volume manufacturing since 2009
- Design Kit established

300 mm Si Photonics process (in qualification)
- ST Microelectronics (Crolles, France)
- Process development started 2012
- Only photonic devices (passive and active)
- Developing photonic device libraries for multiple $\lambda$ ranges
- Design Kit under development
- First results presented at IEDM 2013 (F. Boeuf et al.)
Silicon Photonics: Transceiver Architecture

- Serial Interface
- Digital Control
- 1:4 Optical Splitter
- To Other Channels
- Laser Driver
- Laser
- Single-Mode Waveguide
- SFP In
- HSPM
- TX Control
- ADC
- Monitor PD
- Tap
- Distributed MZI Driver and Calibration Circuit
- Cal.
- PIN
- SFP Out
- SFP Driver
- Receiver
- PD
- Optical Inputs
- Optical Outputs
- SPGC
- PSGC
- TX Control
- ADC
- Monitor PD
- Tap
- Distributed MZI Driver and Calibration Circuit
- Cal.
- PIN
- SFP Out
- SFP Driver
- Receiver
- PD
- Optical Inputs
- Optical Outputs
- SPGC
- PSGC
• Couplers based on diffractive structures: Surface coupling
• Low coupling loss: < 1 dB demonstrated
• Alignment of light source and fiber to Si P couplers:
  – Vision-based pre-alignment
  – Active alignment (w/optical feedback loop for in-situ coupling optimization): very fast < 1 s
Silicon Photonics: Wafer Level Optical Testing

- Based on industry standard TEL Precio prober
- 200 and 300 mm Silicon Photonics wafer testing
- Easy test of single wafers, full cassette & FOUPs
- 4X faster than previous solution for optical sort
- Optical test capability: Gauge R&R: 0.1 dB
- Wafer-scale testing is a work horse for manufacturing and development: Operates ~24/7
- Wafer Level Optical Test technology now licensed to TEL
Silicon Photonics Optical Transceivers: Transmitter

- Mach-Zehnder Modulator built with High-speed Phase Modulators (HSPM) based on carrier depletion:

- Segmented design w/ two voltage rails, digital delays for phase matching and integrated quadrature bias control:
Silicon Photonics Optical Transceivers: Receiver

- SMF Waveguide Photo-detector Interface:

- Receiver: Germanium Photodiode with TIA & LA:

  - Ge Waveguide Photodiode
  - Amplification stages
  - RX Electrical transmitter
  - Differential receiver output

Implants
Germanium
Contact
Input waveguide
Light Source for Silicon Photonics

- Most transceiver applications need the light source to be co-packaged, but Si Photonics also offers ability to use a remote light source
- Luxtera has explored many types of light sources approaches, finally selected a standard InP laser diode in a silicon micro-package

- Incorporates many “lessons learned”:
  - Use a mature InP laser diode
    -> excellent reliability and manufacturing maturity
  - Include an isolator
  - Use efficient coupling scheme into die
  - Wafer level assembly, packaging and test
  - Established burn-in methods
Packaging Si Photonics, example: QSFP AOC

- Laser Micro Package (LaMP)
- Si P Die with LaMP attached
- Si P Die with LaMP and FA attached
Monolithic integration photonics & electronics
• Single chip solution
• Low parasitics between photonic & electronic devices
• More complex manufacturing process
• In some cases not area efficient
• Scaling to advanced electronic nodes is prohibitively expensive

Hybrid integration photonics & electronics
• Multi-chip solution: face-to-face bonding
• Parasitics between photonic & electronic devices (Cu Pi pads)
• Photonics and electronics decoupled
• Efficient use of area
• Flexibility in process node for electronics
• Enables integration 3rd party electronic IP

Monolithic electronic and photonic IC

Electronic IC

Micro bump interconnect

Photonic IC

Wafer Level IC assembly
Luxtera Si P Transceiver: 8x28 Gbps – Optical Engine

**Electronic IC:** 8 TX w/CDRs, 8 RX w/CDRs

- TSMC N28 HPM node
- MZI drivers & TIA/LAs
- E-interface w/ by-passable CDR & programmable signal conditioning
- Digital core w/ MCU & 2-wire communication
- Laser driver
- BIST

**Photonic Die**
- MZIs
- Ge High-Speed photodetectors
- Ge photodiodes for control and monitoring
- BIST
- Photonic assembly features

**Micro-packaged Light Source**

**Photonic IC:** 8 TX + 8 RX, ~500 Photonic Devices

**Input electrical signal after PCBA w/ 10dB loss**

**Output electrical RX eye (CDR on)**
Optical transceiver qualification per Telcordia GR-468-CORE

- Successfully passed full Telcordia qualification on two generations of Si Photonics based AOCs
- Tests included:
  - 2000 hrs Biased dry heat (85C) extended to 5000hrs for informational purposes
  - ESD testing on CMOS die followed by 1000hrs of biased dry heat (85C)
  - 1000hrs biased damp heat (85C, 85% R.H.) extended to 2000hrs for informational purposes
  - 100 cycles of thermal cycling from -40 to 85C extended to 500 cycles for informational purposes.
  - 50 cycles of biased thermal cycling with humidity
  - Human body model and Air & contact discharge ESD testing
  - Mechanical vibration and shock testing (with and without attached test board)
  - Fiber cable flex, twist & tensile strength testing
  - Durability of electrical connector
  - Insertion/extraction force measurements
  - Thermal shock testing (0 to 100C)

Graph showing Worst-case End-Of-Life (2 dB extra jitter penalty) total jitter after 5000 hrs biased dry heat (85C) across 200 lanes in 25 AOC cables (50 modules).
Transmission Medium
• Single mode fiber scales well for high data rates
• Dispersion effects are negligible for reaches under consideration (100-500 m)

Modulation
• Intrinsic modulation bandwidth of carrier depletion devices is ~ 160 GHz
• Practically limited by RC (e.g. ~ 44 GHz), can be optimized.

Reception
• Waveguide photo-detectors allow high bandwidth without sacrificing responsivity
• BW: > 50 GHz (-1V bias)
• Responsivity: 1.1 A/W

Electronic Circuits
• Advanced CMOS nodes (beyond 28 nm) for low power, high speed electronic functions
Scaling Si Photonics: Increasing Density

25 Gbps NRZ

50 Gbps NRZ

100 Gbps PAM4

32x Rate Increase over Current State of the Art

800 Gbps 2λxPAM4 - MCF

200 Gbps 2λxPAM4
## Interconnect Evolution: Example Switch ASIC

|----------------------|--------------------|-----------------------------|

- Traditional MSA compliant pluggable modules and AOCs on card edge
- Considerable SI issues (electrical connectors, long traces on host PCBA) require re-timers.
- Front panel interconnect density limited by module size (physical implementation + module power dissipation)

- Embedded optical transceivers located closer around ASIC
- Shorter traces on PCB alleviate SI issues
- Optical fibers bring IOs to optical connectors on front panel
- Front panel interconnect density limited by size optical connectors
- Very high reliability required

- Optical transceivers co-packaged w/ ASIC
- Minimized electrical interconnect eliminates SI issues
- Optical fibers bring IOs to optical connectors on front panel
- Lowest system power dissipation
- Highest front panel density and smallest potential system form factor
- Very high reliability required
Major power reduction by integrating optics

- MSA Optics
- Embedded Optics
- Integrated Optics

Legend:
- Purple: External Light Source
- Green: Module Optical
- Red: Module Electrical
- Blue: Host Electrical

Graph showing power per 100G (W) for each option.
Photonic Interposer: ASIC with Optical I/O

20 mm x 20 mm ASIC with e.g. 36 100G macros for optical TX/RX I/Os on 30.5 mm x 22 mm photonic interposer

Optical fibers provide high-speed interconnect and provide supply of DC light to transmitters

Heat sink mounted on package

Optical coupler: interfaces between interposer and MT-ferrules

Photonic Interposer w/TSV

Package Substrate:
- high & low speed IO
- power supply and
- mechanical support to interposer

MT-Ferrules as example for pluggable fiber interconnect

Host PCBA
**Higher Data Flux:**
- Data flux is limited by
  - Shelf:
    - Face plate density limited by module/connector size
    - Optical module size also determined by power
  - ASIC: limited by electrical I/Os BGA package
- Solutions:
  - Increase raw data rate
  - Integrate optical I/O with ASIC allowing higher density and lower power dissipation

**Longer Interconnect Reach Required:**
- New architectures for datacenters and HPC require longer interconnect reaches at higher data rates while maintaining low latency
- Web 2.0 data centers and HPC represent large market for long reach optical interconnect solutions
- Long reach at high data rate: single mode fiber only practical solution
Web2.0 / Cloud Data Centers

- Focus on
  - Performance (# petaflops, size and power)
  - Cost (Photonics dominate system BOM cost ~ 66%)
- Equipment is disposable
  - Optimized for application
  - Frequent hardware refresh
- Drive towards disruptive, higher performance hardware
- Interconnect becomes very important (function, power and cost)

Interconnect Requirements for Cloud Data Centers

- Longer reach: ~500 m
- Need scalable fiber infrastructure (data rate and density)
- Low power
- High Reliability
- Low cost

Web 2.0/Cloud: Great opportunity for disruptive technologies

- Significant HW investments
- Enterprise market will adopt later and leverage due to drastic difference in cost and power/bit
Conclusions

• Silicon Photonics has been **in production since 2009**, the first product was an 4x10 G AOC [now sold by Molex]

• **Cloud datacenter** build out drives single mode silicon photonics optical interconnect applications, where it is now already deployed

• Currently in development and qualification of Nx100G parallel single mode products (**PSM4 MSA**) in various form factors

• Work has already started on **400 G and associated low-cost duplex 100G transceiver products** using a combination of higher baud rate, PAM-N and WDM

• Power reduction drives closer integration, first by use of Embedded Optical Modules, later by direct integration with ASICs by a **Photonically Enabled Silicon Interposer** (addition of TSV to Si Photonics flow)
This presentation shows the work of the entire Luxtera team, their contributions are greatly acknowledged.

Thank you for your interest.