3D in the Deep Submicron Era

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Customers Are Asking for More

- More than 2X today’s logic capacity...
- Many more high-speed serial transceivers...
- More integration of processing elements and memory
Why 3D? The 3 Cs of 3D

- Connectivity
- Capacity
- Crossovers
Connectivity: Enables High Bandwidth, Low Power Die-to-Die Communication

100x bandwidth/watt advantage over conventional methods

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### Capacity Beyond Moore’s Law

<table>
<thead>
<tr>
<th>Big Single Monolithic Die</th>
<th>Multiple Small Die Slices</th>
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</thead>
</table>

- **✓ Greater capacity, faster yield ramp**
“Crossover SoCs” with Heterogeneous Die

- Mixed functions
- Mixed processes
The Progression of 3D Technology

Traditional MCM/PCB
- Analog
- RF
- Passive
- Logic
- Memory

Flipchip + wire bond

Silicon Interposer 2.5D
- 2.5D side-by-side integration with TSVs & silicon interposer

Full 3D
- Vertical stacking with memory & logic

Source: TSMC
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Technical Challenges Posed by 3D

3D – Active on Active

Vertical Die Stacking

Active → RAM
Active → Logic

Microbump / TSV

Thermal

corner
center

TSV-Induced Device Stress

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Technical Challenges Posed by 2.5D

2.5D – Active on Passive

<table>
<thead>
<tr>
<th>Side-by-side Die Placement</th>
</tr>
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<tbody>
<tr>
<td>Active</td>
</tr>
<tr>
<td>Passive</td>
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</table>

- **Microbump / TSV**
- **Thermal**
- **TSV-Induced Device Stress**

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Example: Xilinx FPGA Based on Stacked Silicon Interconnect Technology

FPGA Slices Side-by-Side

ASMBL-optimized FPGA slice

Silicon Interposer:
> 10K routing connections between slices
~ 1ns latency
2.5D Delivers Resource-Rich FPGAs

Largest Device with Transceivers

Xilinx

With 2.5D

Without 2.5D

Logic Cells

2.0M

1.5M

1.0M

0.5M

0.0M

90nm

65nm

40nm

28nm

3.5x

2x
Assembly Options Considered

TSV via and Microbumps
Source: Xilinx, TSMC, Amkor

Die to Die
1. M. Reflow + CUF
   - Die to Die Attach
   - Reflow
   - Capillary Underfill
   - Die Stack to Substrate
   - Reflow
   - Capillary Underfill
   - Final Test

2. TC Bond + CUF
   - Die to Die TC Bond
   - Capillary Underfill
   - Die Stack to Substrate
   - Reflow
   - Capillary Underfill
   - Final Test

3. TC Bond + NCP
   - Die to Die TC + NCP
   - Capillary Underfill
   - Die Stack to Substrate
   - Reflow
   - Capillary Underfill
   - Final Test

Die to Wafer
1. TC Bond + CUF
   - Die to Wafer TC
   - Capillary Underfill
   - Die Stack to Substrate
   - Reflow
   - Capillary Underfill
   - Final Test

2. TC Bond + NCP
   - Die to Wafer TC + NCP
   - Capillary Underfill
   - Die Stack to Substrate
   - Reflow
   - Capillary Underfill
   - Final Test
Role of the Supply Chain in 3D

Xilinx SSI Supply Chain

FPGA, Interposer, & Package Design

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28nm FPGA & Interposer

tsmc

Package Substrate

IBI IBIDEN

μBump, Die separation
CoC attach, & Assembly

Amkor Technology

Final Test of Packaged Part

XILINX
3D Call-to-Action: Develop & Evolve Standards

- **Design enablement**
  - Models
  - 3D Process Development Kit

- **Manufacturing standards**
  - DFM rules for TSV, microbump (AR, keep-out)
  - Materials TSV, u-bump
  - Thermal budget

- **Test**
  - Test HW
  - KGD method
  - u-bump probing

- **Interoperability of silicon between fabs**
  - Shipping methods

- **Chip-to-chip Interfaces**
Summary

✓ 3D IC technology
  – Significantly changing the semiconductor landscape

✓ Challenges remain
  – Technical and business-related

✓ 2.5D IC technology
  – An important & lower risk path

✓ 3D Call to Action
  – How will the industry step up to resolve key issues?