Motivation for 3D SiP

- Functional Diversification (More than Moore)
- Analog II, Power, Passive, Sensors, Biocomps
- Interfacing with people and environment
- Non-digital content (System-in-package (SiP))
- Information Processing
- Digital content (System-on-chip (SoC))
- Beyond CMOS
Application Areas for Energy Efficient Smart Electronic 3D Systems

- Safety & Security
- Transport & Mobility
- IT & Communication
- Ambient Assisting Living & Health Care
- Energy Management & Harvesting
- Lighting
- Green Environment Monitoring
- Automation

Heterogeneous System Integration

SENS - DATA PROCESSING - ACTING - COMMUNICATION

Environment

- Sensors
- Actuators
- Power Management
- IC, MPU, Memory, Passives
- wireless RF

Network

- Data transmission

Physical, Chemical, Biological Data

Energy

RF IC, MPU, Memory, Passives
Driving Forces for 3D Heterogeneous Integration - SiP

Form Factor & Miniaturization
- Reduced volume and weight
- Reduced footprint

Performance
- Improved integration density
- Reduced interconnect length
- Improved transmission speed
- Reduced power consumption

Heterogeneous Integration & Functionality
- Mixed functional integration
- MEMS, Optical, AD SP, Transceiver

Manufacturing Cost Reduction

Smart 3D Systems using TSV Technology

3D TSV Packaging Market Value

Source: Yole
There are many challenges and new architectures in packaging. These challenges increase as we deal with 3D and SiP packaging.

These challenges include:

- Complex design architecture
- Thermal Management
- Power integrity
- Test
- Reliability
  - Stress management (die, layer, board)
  - TCE mismatch
- Standardization

Ref. B Chen

3D System Integration: Key Enabling Technologies

- 3D SiP Architecture
- Design - electrical, thermal (DfT, DfM, DfR)
- TSV Formation
- Interposer with multilayer RDL (FS/BS)
- Passive Device Integration
- Interconnect Formation (electrical, optical)
- Thin Wafer Handling
- Temporary and permanent Wafer Bonding
- Assembly & 3D Stack Formation
- Heterogeneous Device Integration
- Housing
- Test
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TSV Formation

Technology:
- TSV Etching: RIE (Bosch process)
- TSV Isolation: SiO₂ (CVD, therm.)
- Barrier/Seed: PVD, CVD, Wet
- TSV Filling: Cu-ECD, W-CVD, pSi

Challenges:
- HASR TSV (etch, uniformity, fill, yield)
- Design (rules, CAD tools)
- Metrology, test
- Reliability (uniformity, yield)
- Cost (throughput, ...)

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Temp. Bonding / De-Bonding

Technology:
- UV / Laser
- Thermal slide
- Solvent
- Mechanical peel-off

Challenges:
- TTV uniformity
- High topology
- Temperature and chemical stability
- Easy de-bonding
- Low residue
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**Chip Interconnection (D2D, D2W, D2IP, IP2P)**

**Technology:**
- Solder, IMC, Cu-Cu, Nano-Interconnects
- Bonding (reflow, TC)
- Stacking (D2W, D2W, W2W)
- Interconnect structure (Cu, ...)

**Challenges:**
- Low temperature bonding
- Bonding on carrier vs. wafer
- Reliability, test, repair
- Productivity, throughput, yield

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**Through Silicon Via Interposer / HD-Multi Device Carrier**

*Silicon Interposer with Cu-TSV, multi layer Cu redistribution layer and FC bonded circuit devices*

- Cu-TSV (> 10000/cm²) (8“)
- High density Multi-Layer Redistribution (4 Layer Cu)
- Flip chip compatible IO-Pads
- Cu-Pillar Bumps
- SnAg Micro Solder Bumps
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**TSV-Interposer #2**

Silicon Interposer Apps #1:
- high TSV count (>10000/vm²)
- high density TSV (5-10 μm)
- small pitch (50-20 μm)
- high density Line/Space
- multilayer front/back side
- electrical & optical Interconnect

Silicon Interposer Apps #2:
- med. TSV count
- med. TSV (10-20 μm), pitch (>100 μm)
- ASR (5-15)
- multilayer front/back side
- MEMS integration
- Cu pillar interface to board/package

**Future Potential:**
- passive device integration
- optical interconnect
- cooling
- heterogeneous device integration (e.g. TX, MEMS)
- e.g. thin chip integration

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**3D Wafer Level System Integration (Examples)**

TPM 3D ASIC+TX+MEMS

WL Camera (tapered TSV)

TSV Interposer (GP+MEM)

Image Sensor (tapered TSV)

Image Sensor (Sensor+SP)

TCI (Sensor+ASIC+TX)
IZM / ASSID develops leading edge technologies for 3D WL System-Integration and provides solutions ready for product integration to industrial partners.

IZM / ASSID offers capacity in R&D and process development and prototyping on a state-of-the-art 200/300mm process line for WL packaging and 3D WL system integration.

Fraunhofer IZM vision is to integrate heterogeneous chip functionalities into one WL Package using enhanced 3D integration, assembly and interconnect technologies.
THANK YOU FOR YOUR ATTENTION

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